

<<60GHz CMOS锁相环技术>>

图书基本信息

书名：<<60GHz CMOS锁相环技术>>

13位ISBN编号：9787030344762

10位ISBN编号：7030344766

出版时间：2012-6

出版时间：科学出版社

作者：Hammad M.Cheema、Reza Mahmoudi、Arthur H.M.van Roermund

页数：197

字数：289000

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：<http://www.tushu007.com>

<<60GHz CMOS锁相环技术>>

内容概要

近年来，毫米波尤其是60GHz频率段的高数据无线传输应用已经备受关注。而在毫米波CMOS电路设计时布线和测量所面临的问题需要科研人员认真解决。60GHz CMOS锁相环技术重点阐述了60GHz无线收发器技术面临的技术挑战，并提出了解决方案。

<<60GHz CMOS锁相环技术>>

书籍目录

1 Introduction
 2 Synthesizer System Architecture
 2.1 IEEE 802.15.3c Channelization
 2.2 60 GHz Frequency Conversion Techniques
 2.3 Proposed PLL Architecture: Flexible, Reusable, Multi-frequency
 2.3.1 Utilization in WiComm Project
 2.4 System Analysis and Design
 2.4.1 Phase-Lock Loop Basics
 2.4.2 Frequency Planning
 2.4.3 Synthesizer Parameters
 2.5 System Simulations
 2.6 Target Specifications
 2.7 Summary
 3 Layout and Measurements at mm-Wave Frequencies
 3.1 Layout Problems and Solutions
 3.1.1 Impact of Parasitics
 3.1.2 Mismatch Due to Layout Asymmetry and Device Orientation
 3.1.3 Substrate Losses
 3.1.4 Cross Talk Shielding and Grounding
 3.2 Measurement Setups
 3.2.1 Dedicated Instrumentation
 3.2.2 Calibration and De-embedding
 3.2.3 Stability and Repeatability
 3.3 Conclusions
 4 Design of High Frequency Components
 4.1 Prescaler
 4.1.1 Overview and Comparison of Prescaler Architectures
 4.1.2 35 GHz Static Frequency Divider
 4.1.3 40 GHz Divide-by-2 ILFD
 4.1.4 60 GHz Divide-by-3 ILFD
 4.1.5 Monolithic Transformer Design and Measurement
 4.1.6 Dual-Mode (Divide-by-2 and Divide-by-3) LLFD
 4.1.7 ILFD Figure-of-Merit (FOM)
 4.1.8 Summary
 4.2 Voltage Controlled Oscillator
 4.2.1 Overview of VCO Architectures
 4.2.2 Theoretical Analysis of LC-VCOs
 4.2.3 40 GHz LC VCO
 4.2.4 60 GHz Actively Coupled I-Q VCO
 4.2.5 60 GHz Transformer Coupled I-Q VCO
 4.2.6 Dual-Band VCO for 40 and 60 GHz
 4.3 Synthesizer Front-Ends
 4.3.1 40 GHz VCO and Divide-by-2 ILFD
 4.3.2 60 GHz VCO and Divide-by-3 ILFD
 4.4 Conclusions
 5 Design of Low Frequency Components
 5.1 Feedback Division
 5.1.1 CML Based Divider Chain
 5.1.2 Mixer Based Division
 5.2 Phase-Frequency Detector, Charge-Pump and Loop Filter
 5.3 Conclusions
 6 Synthesizer Integration
 6.1 Synthesizer for 60 GHz Sliding-IF Frequency Conversion
 6.1.1 Comparison to Target Specifications
 6.2 Synthesizer with Down-Conversion Mixer in Feedback Loop
 6.3 Dual-Mode Synthesizer
 6.4 Conclusions
 7 Conclusions
 Appendix
 Appendix AA Travelling Wave Divider Simulation Results
 Appendix BB LC-VCOs Theory
 References

<<60GHz CMOS锁相环技术>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>