

<<高速CMOS电路设计>>

图书基本信息

书名：<<高速CMOS电路设计>>

13位ISBN编号：9787115195982

10位ISBN编号：7115195986

出版时间：1970-1

出版时间：人民邮电

作者：(美)萨瑟兰德//斯普劳尔//哈里斯

页数：239

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：<http://www.tushu007.com>

<<高速CMOS电路设计>>

前言

The method of logical effort is a way of thinking about delay in Mos circuits. It seeks to determine quickly a circuits maximum possible speed and how to achieve it. It provides insight into how both the sizes of different transistors and the circuit topology itself affect circuit delay. We offer two new names for causes of delay in Mos circuits , electrical effort and logical effort. The similarity of these names reflects a remarkable symmetry between the effort required to drive an electrical load and the effort required to perform a logic function; the two forms of effort present identical and inter- changeable sources of delay. Identifying these concepts leads to a formulation that simplifies circuit analysis and allows a designer to analyze alternative circuit designs quickly. Electrical effort is a new name for the problem overcome by electrical gain. It has long been known that the fastest driver for a large electrical load is a multistage amplifier whose gain is distributed among stages of exponentially increasing size. Thinking of what amplifiers do as compensating for electrical effort paves the way to understanding how they similarly compensate for logical effort.

<<高速CMOS电路设计>>

内容概要

《高速CMOS电路设计Logical Effirt方法(英文版)》讲述如何获得高速CMOS电路，这正是高速集成电路设计师们渴望获得的技术。

在设计中，我们往往面对无数的选择，《高速CMOS电路设计Logical Effirt方法(英文版)》将告诉我们如何将这些选择变得更容易和更有技巧。

《高速CMOS电路设计Logical Effirt方法(英文版)》提供了一个简单而普遍有效的方法，用于估计拓扑、电容等因素造成的延迟。

《高速CMOS电路设计Logical Effirt方法(英文版)》实用性强，适合集成电路设计师以及相关专业的师生。

<<高速CMOS电路设计>>

作者简介

Ivan Sutherland, 著名计算机科学家。
因对计算机图形学和电子设计领域的开创性贡献先后获得1988年图灵奖和1998年冯·诺依曼奖。
美国科学院院士、美国工程院院士和ACM会士。
现任Sun公司副总裁。

Bob Sproull, 著名计算机科学家, 美国工程院院士。
现为Sun公司副总裁兼研究中心主任。
Sutherland的长期合作者。

David Harris Harvey Mudd, 学院副教授。
曾参与Intel安腾和奔腾II的电路设计。
除本书外, 他还与Weste合著了名作CMOSVLSI Design: A Circuits and Systems Perspective。

<<高速CMOS电路设计>>

书籍目录

1 The Method of Logical Effort1.1 Introduction1.2 Delay in a Logic Gate1.3 Multistage Logic Networks1.4 Choosing the Best Number of Stages1.5 Summary of the Method1.6 A Look Ahead1.7 Exercises2 Design Examples2.1 The AND Function of Eight Inputs2.2 Decoder2.3 Synchronous Arbitration2.4 Summary2.5 Exercises3 Deriving the Method of Logical Effort3.1 Model of a Logic Gate3.2 Delay in a Logic Gate3.3 Minimizing Delay along a Path3.4 Choosing the Length of a Path3.5 Using the Wrong Number of Stages3.6 Using the Wrong Gate Size3.7 Summary3.8 Exercises4 Calculating the Logical Effort of Gates4.1 Definitions of Logical Effort4.2 Grouping Input Signals4.3 Calculating Logical Effort4.4 Asymmetric Logic Gates4.5 Catalog of Logic Gates4.6 Estimating Parasitic Delay4.7 Properties of Logical Effort4.8 Exercises5 Calibrating the Model5.1 Calibration Technique5.2 Designing Test Circuits5.3 Other Characterization Methods5.4 Calibrating Special Circuit Families5.5 Summary5.6 Exercises6 Asymmetric Logic Gates6.1 Designing Asymmetric Logic Gates6.2 Applications of Asymmetric Logic Gates6.3 Summary6.4 Exercises7 Unequal Rising and Falling Delays7.1 Analyzing Delays7.2 Case Analysis7.3 Optimizing CMOS P/N Ratios7.4 Summary7.5 Exercises8 Circuit Families8.1 Pseudo-NMOS Circuits8.2 Domino Circuits8.3 Transmission Gates8.4 Summary8.5 Exercises9 Forks of Amplifiers9.1 The Fork Circuit Form9.2 How Many Stages Should a Fork Use?9.3 Summary9.4 Exercises10 Branches and Interconnect10.1 Circuits That Branch at a Single Input10.2 Branches after Logic10.3 Circuits That Branch and Recombine10.4 Interconnect10.5 A Design Approach10.6 Exercises11 Wide Structures11.1 An n-input AND Structure11.2 An n-input Muller C-element11.3 Decoders11.4 Multiplexers11.5 Summary11.6 Exercises12 Conclusions12.1 The Theory of Logical Effort12.2 Insights from Logical Effort12.3 A Design Procedure12.4 Other Approaches to Path Design12.5 Shortcomings of Logical Effort12.6 Parting WordsAPPENDICESA Cast of CharactersB Reference Process ParametersC Solutions to Selected ExercisesBIBLIOGRAPHYINDEX

章节摘录

To set the context of the problems addressed by logical effort, we begin by reviewing a simple integrated circuit design flow. We will see that topology selection and gate sizing are key steps of the flow. Without a systematic approach, these steps are extremely tedious and time-consuming. Logical effort offers such an approach to these problems. Figure I. 1 shows a simplified chip design flow illustrating the logic, circuit, and physical design stages. The design starts with a specification, typically in textual form, defining the functionality and performance targets of the chip. Most chips are partitioned into more manageable blocks so that they may be divided among multiple designers and analyzed in pieces by CAD tools. Logic designers write register transfer level (RTL) descriptions of each block in a language like Verilog or VHDL and simulate these models until they are convinced the specification is correct. Based on the complexity of the RTL descriptions, the designers estimate the size of each block and create a floorplan showing relative placement of the blocks. The floorplan allows wire-length estimates and provides goals for the physical design. Given the RTL and floorplan, circuit design may begin. There are two general styles of circuit design: custom and automatic. Custom design trades additional human labor for better performance. In a custom methodology, the circuit designer has flexibility to create cells at a transistor level or choose from a library of predefined cells. The designer must make many decisions: Should I use static CMOS, transmission gate logic, domino circuits, or other circuit families? What circuit topology best implements the functions specified in the RTL?

<<高速CMOS电路设计>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>