

<<现代处理器设计>>

图书基本信息

书名：<<现代处理器设计>>

13位ISBN编号：9787302153573

10位ISBN编号：7302153574

出版时间：2007-8

出版时间：清华大学

作者：谢

页数：642

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：<http://www.tushu007.com>

<<现代处理器设计>>

内容概要

本书是关于处理器设计的最新、最权威教材，主要论述了：（1）处理器的设计方法和原理；（2）流水线技术；（3）主存与I/O系统；（4）超标量组织与技术；（5）POWERPC 620和Intel P6等示例；（6）超标量处理器设计；（7）先进的指令流技术、存储器数据流技术；（8）多线程技术等。

本书适合作为计算机及相关专业的“处理器设计”课程的教材，也是有关专业人员很有价值的参考用书。

作者简介： John Paul Shen is the Director of Intel's Microarchitecture Research Lab (MRL), providing leadership to about two-dozen highly skilled researchers located in Santa Clara, CA; Hillsboro, OR; and Austin, TX. MRL is responsible for developing innovative microarchitecture techniques that can potentially be used in future microprocessor products from Intel. MRL researchers collaborate closely with microarchitects from product teams in joint advanced-development efforts. MRL frequently hosts visiting faculty and Ph.D. interns and conducts joint research projects with academic research groups. Prior to joining Intel in 2000, John was a professor in the electrical and computer engineering department of Carnegie Mellon University, where he headed up the CMU Microarchitecture Research Team (CMuART). He has supervised a total of 16 Ph.D. students during his years at CMU. Seven are currently with Intel, and five have faculty positions in academia. He won multiple teaching awards at CMU. He was an NSF Presidential Young Investigator. He is an IEEE Fellow and has served on the program committees of ISCA, MICRO, HPCA, ASPLOS, PACT, ICCD, ITC, and FFCS. He has published over 100 research papers in diverse areas, including fault-tolerant computing, built-in self-test, process defect and fault analysis, concurrent error detection, application-specific processors, performance evaluation, compilation for instruction-level parallelism, value locality and prediction, analytical modeling of superscalar processors, systematic microarchitecture test generation, performance simulator validation, precomputation-based prefetching, database workload analysis, and user-level helper threads. John received his M.S. and Ph.D. degrees from the University of Southern California, and his B.S. degree from the University of Michigan, all in electrical engineering. He attended Kimball High School in Royal Oak, Michigan. He is happily married and has three daughters. His family enjoys camping, road trips, and reading The Lord of the Rings.

<<现代处理器设计>>

作者简介

作者：(美国)谢 等

<<现代处理器设计>>

书籍目录

Table of Contents

Additional Resources

Preface

1 Processor Design 1.1 The Evolution of Microprocessors 1.2 Instruction Set Processor Design 1.2.1 Digital Systems Design 1.2.2 Architecture, Implementation, and Realization 1.2.3 Instruction Set Architecture 1.2.4 Dynamic-Static Interface 1.3 Principles of Processor Performance 1.3.1 Processor Performance Equation 1.3.2 Processor Performance Optimizations 1.3.3 Performance Evaluation Method 1.4 Instruction-Level Parallel Processing 1.4.1 From Scalar to Superscalar 1.4.2 Limits of Instruction-Level Parallelism 1.4.3 Machines for Instruction-Level Parallelism 1.5 Summary

2 Pipelined Processors 2.1 Pipelining Fundamentals 2.1.1 Pipelined Design 2.1.2 Arithmetic Pipeline Example 2.1.3 Pipelining Idealism 2.1.4 Instruction Pipelining 2.2 Pipelined Processor Design 2.2.1 Balancing pipeline Stages 2.2.2 Unifying Instruction Types 2.2.3 Minimizing Pipeline Stalls 2.2.4 Commercial Pipelined Processors 2.3 Deeply Pipelined Processors 2.4 Summary

3 Memory and I/O Systems 3.1 Introduction 3.2 Computer System Overview 3.3 Key Concepts: Latency and Bandwidth 3.4 Memory Hierarchy 3.4.1 Components of a Modern Memory Hierarchy 3.4.2 Temporal and Spatial Locality 3.4.3 Caching and Cache Memories 3.4.4 Main Memory 3.5 Virtual Memory Systems 3.5.1 Demand Paging 3.5.2 Memory Protection 3.5.3 Page Table Architectures 3.6 Memory Hierarchy Implementation 3.7 Input/Output Systems 3.7.1 Types of I/O Devices 3.7.2 Computer System Busses 3.7.3 Communication with I/O Devices 3.7.4 Interaction of I/O Devices and Memory Hierarchy 3.8 Summary

Superscalar Organization 4.1 Limitations of Scalar Pipelines 4.1.1 Upper Bound on Scalar Pipeline Throughput 4.1.2 Inefficient Unification into a Single Pipeline 4.1.3 Performance Lost Due to a Rigid Pipeline 4.2 From Scalar to Superscalar Pipelines 4.2.1 Parallel Pipelines 4.2.2 Diversified Pipelines 4.2.3 Dynamic Pipelines 4.3 Superscalar Pipeline Overview 4.3.1 Instruction Fetching 4.3.2 Instruction Decoding 4.3.3 Instruction Dispatching 4.3.4 Instruction Execution 4.3.5 Instruction Completion and Retiring 4.4 Summary

5 Superscalar Techniques 5.1 Instruction Flow Techniques 5.1.1 Program Control Flow and Control Dependences 5.1.2 Performance Degradation Due to Branches 5.1.3 Branch Prediction Techniques 5.1.4 Branch Misprediction Recovery 5.1.5 Advanced Branch Prediction Techniques 5.1.6 Other Instruction Flow Techniques 5.2 Register Data Flow Techniques 5.2.1 Register Reuse and False Data Dependences 5.2.2 Register Renaming Techniques 5.2.3 True Data Dependences and the Data Flow Limit6

6 The PowerPc 6207 Intel's P6 Microarchitecture

8 Survey of Superscalar Processors

9 Advanced Instruction Flow Techniques

10 Advanced Register Data Flow Techniques

11 Executing Multiple Threads

Index

<<现代处理器设计>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>